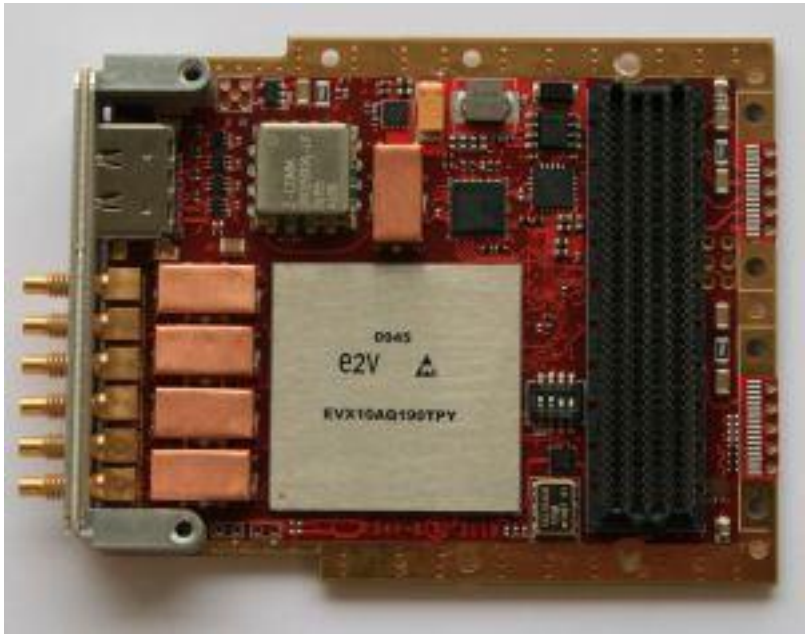
# FMC122/FMC125/FMC126
## User Manual

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# Revision History

| Date | Revision | Revision |
|---|---|---|
| 2010-04-13 | Initial release | 1.0 |
| 2010-09-08 | Added signal description to pin out tables. | 1.1 |
| 2010-09-15 | Added I2C/SPI architecture description. Added monitoring device parameters. | 1.2 |
| 2010-09-20 | Updated block diagram | 1.3 |
| 2010-10-12 | Updated address | 1.4 |
| 2011-03-01 | Added MICTOR connector references | 1.5 |
| 2011-03-09 | Added coax connector type specification | 1.6 |
| 2011-04-14 | Added FMC connector type specification.<br>Updated trigger input specification. | 1.7 |
| 2011-08-01 | Update external clock/reference input level. | 1.8 |
| 2011-09-09 | Added optional clock output specification.<br>Added I2C signals to the pin-out tables. | 1.9 |
| 2011-10-04 | Corrected internal clock specification and clock tree diagram.<br>Added DIP-Switch description. | 1.10 |
| 2012-01-10 | Updated power consumption.<br>Updated performance numbers.<br>Added FAN control details. | 1.11 |
| 2012-10-08 | Added changes between revision 1 and revision 2 boards | 1.12 |
| 2013-08-17 | Changed the number of channels available on FMC122 | 1.13 |
| 2014-03-06 | Changed input power level of external reference | 1.14 |
| 2014-04-07 | Revised some descriptions and fixed typos. | 1.15 |
| 2014-06-19 | Changed pin 20 into “shell” in Table 2. HDMI connector pin out. | 1.16 |
| 2015-04-30 | Updated description of front panel HDMI I/O, section 4.1.3 | 1.17 |

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# 1 Acronyms and related documents

## 1.1 Acronyms

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| DDR | Double Data Rate |
| EPROM | Erasable Programmable Read-Only Memory |
| FBGA | Fineline Ball Grid Array |
| FMC | FPGA Mezzanine Card |
| FPGA | Field Programmable Gate Array |
| JTAG | Join Test Action Group |
| LED | Light Emitting Diode |
| LVTTL | Low Voltage Transistor Logic level |
| LSB | Least Significant Bit(s) |
| LVDS | Low Voltage Differential Signaling |
| MGT | Multi-Gigabit Transceiver |
| MSB | Most Significant Bit(s) |
| PCB | Printed Circuit Board |
| PLL | Phase-Locked Loop |
| PSSR | Power Supply Rejection Ratio |

**Table 1: Glossary**

## 1.2 Related Documents

- FPGA Mezzanine Card (FMC) standard ANSI/VITA 57.1-2008
- Datasheet AD9517-1, E2V
- Datasheet EV8AQ160, E2V
- Datasheet EV10AQ190, E2V
- Datasheet ADT7411 Rev B, Analog Devices
- Datasheet SC18IS602B Rev 04, NXP

# 2 General description

The FMC125/FMC126 is a four channel 1.25Gsps ADC FMC daughter card. The card provides four 8-bit (FMC125) or 10-bit (FMC126) ADC channels that enable simultaneous sampling of four, two, or one channel at a maximum sample rate of 1.25Gsps, 2.5Gsps, or 5Gsps respectively. The FMC122 is a low pin count variant supporting 2 channels at 1.25Gsps or 1 channel at 2.5Gsps maximum sample rate.

The sample clock can be supplied externally through a coax connection or supplied by an internal clock source (optionally locked to an external reference). The clock tree enables cascading of multiple boards for phase-locked sampling. Additionally, a trigger input for customized sampling control is available.

The FMC12x daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1). The card has a high-pin count connector, front panel I/O, and can be used in a conduction-cooled environment.

The design is based on E2V's 8-bit EV8AQ160 (FMC122/FMC125) or 10-bit EV10AQ190 (FMC126) Quad 1.25Gsps ADC with DDR LVDS outputs. The analog signal inputs are available on the front panel on coax connections and have individual calibration circuits for fine-tuning of gain, offset, and phase.

The FMC12x allows flexible control on clock source, sampling frequency, and calibration through serial $I^2C$ communication. Furthermore, the card is equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions or protect the card from overheating.

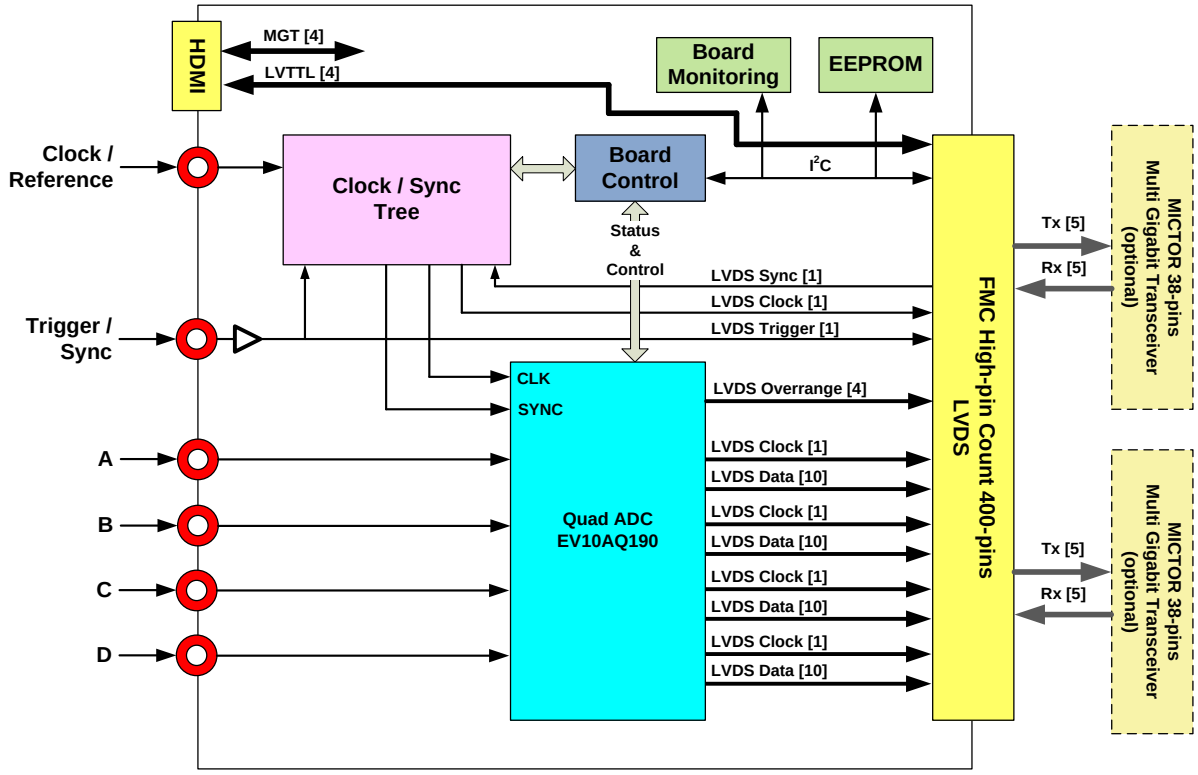


**Figure 1: FMC126 block diagram**

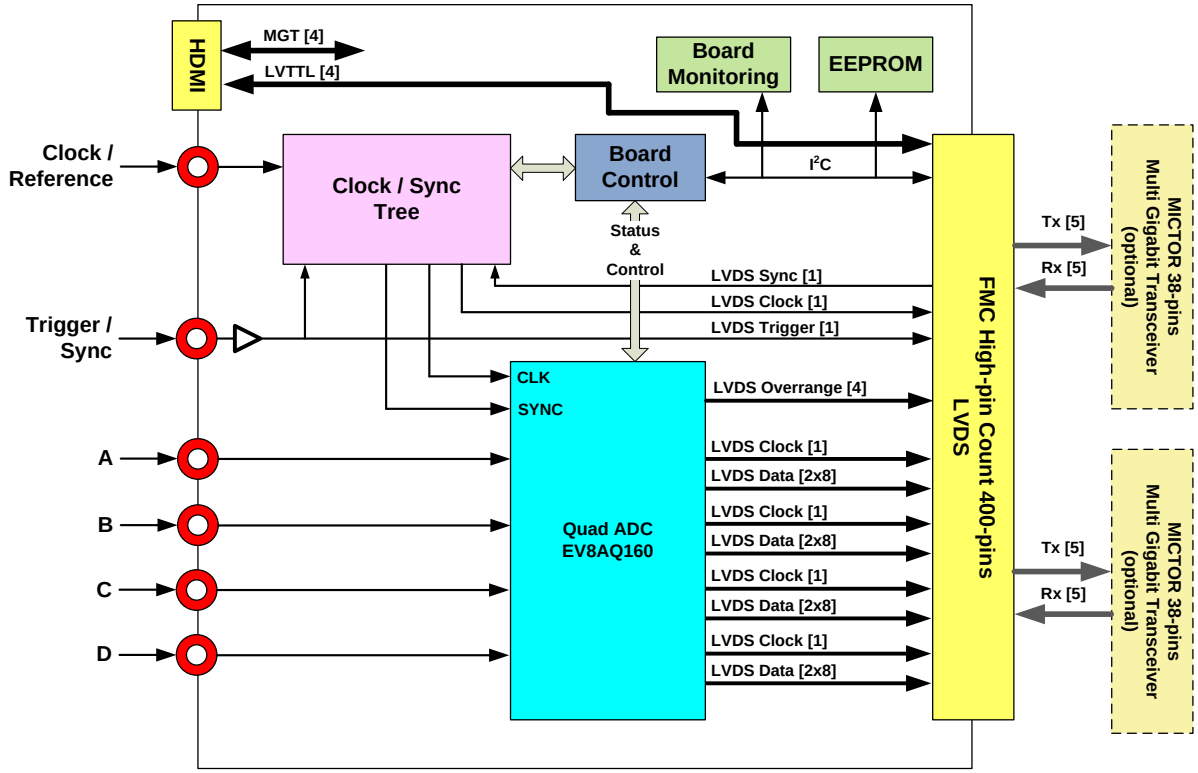


**Figure 2: FMC125 block diagram**

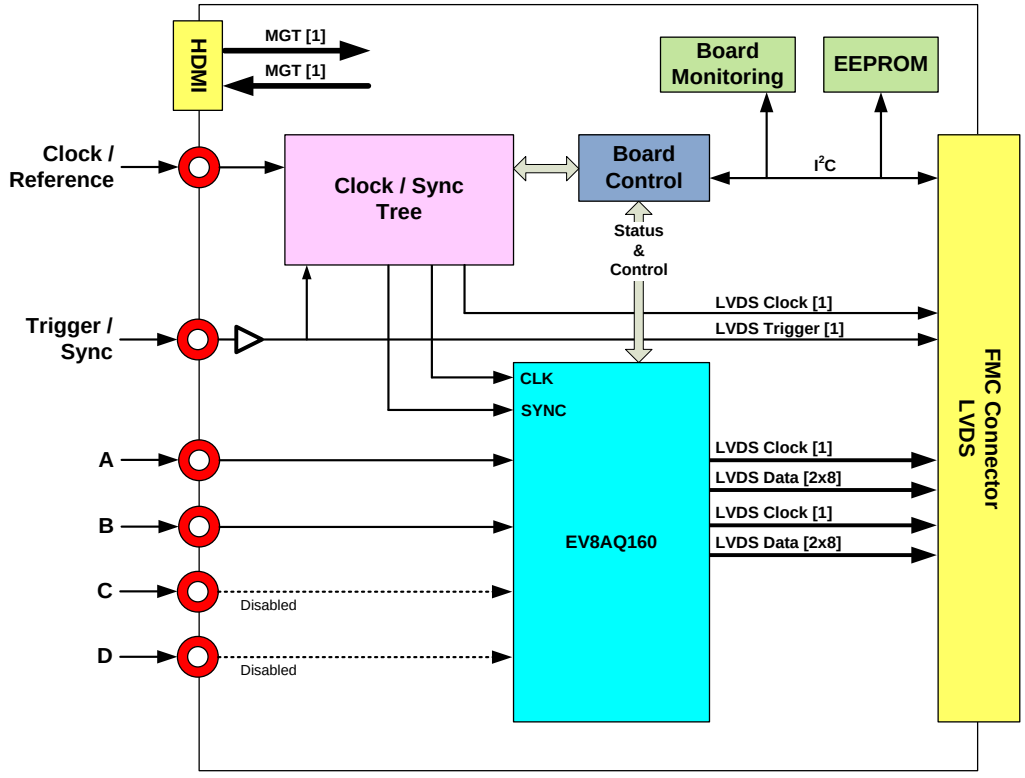


**Figure 3: FMC122 block diagram**

# 3 Installation

## 3.1 Requirements and handling instructions

- The FMC12x daughter card must be installed on a carrier card compliant to the FMC standard.
- The FMC carrier card must support the high-pin count connector (400-pins) for FMC125/FMC126 and may be installed on a low-pin count connector for FMC122.
- The carrier card must support VADJ/VIO_B voltage of +2.5V (LVDS support) for FMC12X revision 1. The carrier card can support VADJ/VIO_B voltage range of 1.65V to 3.3V for FMC12X revision 2, but typically VADJ will be 1.8V or 2.5V for LVDS operation.
- Do not flex the board and prevent electrostatic discharges by observing ESD precautions when handling the card.

## 3.2 LVDS requirements

The FMC12x features parallel DDR LVDS outputs. The FMC122/FMC125 has a 1:2 DMUX feature. In 1:2 DMUX mode, eight 8-bit LVDS busses run at a maximum of 625Mbps each. The FMC126 does not offer a DMUX mode and has four 10-bit busses running at a maximum of 1.25Gbps each.

The FMC12x can output a training pattern on the LVDS outputs to enable phase alignment on the carrier card.

**It should be noted that successful implementation of LVDS connections running at 1.25Gbps (FMC126) highly depends on carrier board design and layout.**

# 4 Design

## 4.1 Phycisal specifications

### 4.1.1 Board Dimensions

The FMC12x card complies with the FMC standard known as ANSI/VITA 57.1. The card is a single-width, conduction-cooled mezzanine module (with region 1 and front panel I/O). The front area holds connectors that might conflict with the front rib keep out area.

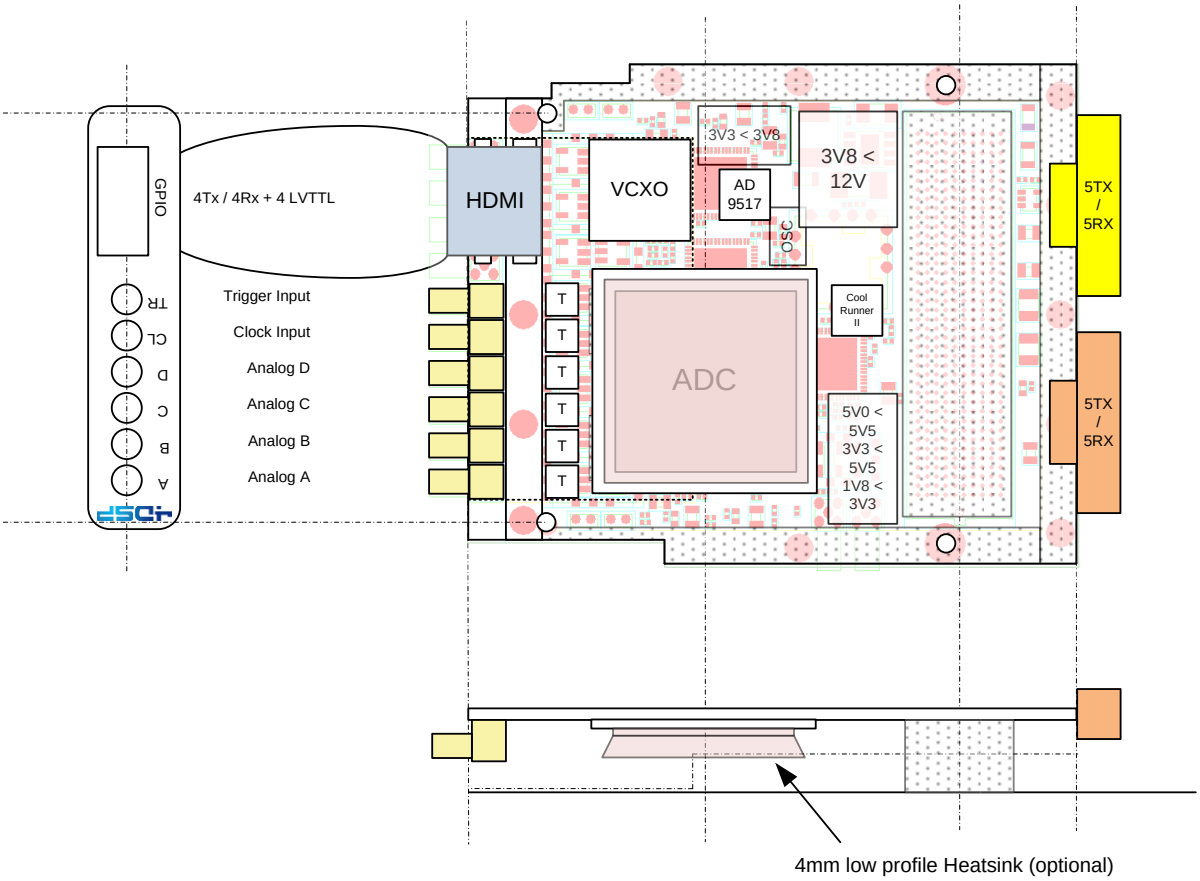


**Figure 4 : FMC122/FMC125/FMC126 dimensions**

### 4.1.2 Front panel

There are six coax connectors available from the front panel. From top to bottom; 1st analog input (A), 2nd analog input (B), 3rd analog input (C), 4th analog input (D), clock input (CL), trigger input (TR).

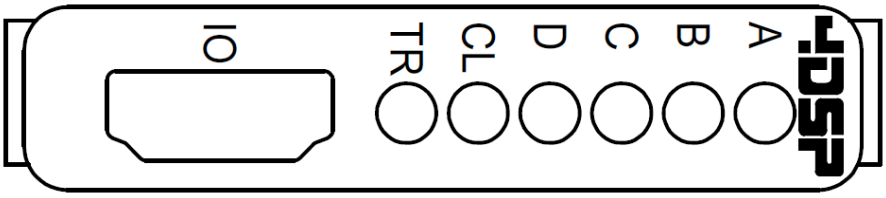


**Figure 5: Bezel drawing**

### 4.1.3 Front panel HDMI I/O

The 19-pins HDMI connector on the front panel (IO) holds four Multi-gigabit transceivers (two Tx pairs / two Rx pairs) and 4x LVTTL I/O (5V tolerant). Contact 4DSP for other configurations.

| Pin Number | Signal Name | Pin Number | Signal Name |
|---|---|---|---|
| **1** | DP_M2C_P<0> | **SHELL** | GND |
| **2** | Shield | **19** | N.C. |
| **3** | DP_M2C_N<0> | **18** | N.C. |
| **4** | DP_M2C_P<1> | **17** | N.C. |
| **5** | Shield | **16** | FRONT_IO<1> |
| **6** | DP_M2C_N<1> | **15** | FRONT_IO<0> |
| **7** | DP_C2M_P<2> | **14** | FRONT_IO<3> |
| **8** | Shield | **13** | FRONT_IO<2> |
| **9** | DP_C2M_N<2> | **12** | DP_C2M_N<3> |
| **10** | DP_C2M_P<3> | **11** | Shield |

**Table 2. HDMI connector pin out**

#### 4.1.3.1 Multi-gigabit transceivers

Two Tx pairs and two Rx pairs of multi-gigabit transceivers connect directly from the HDMI connector to the FMC connector. Refer to Table 2 for the pin locations on the HDMI connector. The signal names match with AV57.1:

- DP_M2C_P/N0 and DP_M2C_P/N1 are mezzanine to carrier pairs and are inputs on the HDMI connector
- DP_C2M_P/N2 and DP_C2M_P/N3 are carrier to mezzanine pairs and are outputs of the HDMI connector

**Note:** the DP_C2M_P/N pairs start with pair number 2 instead of 0. By default, the FMC122 (LPC) only supports the DP_M2C_P/N0 pair.

The transceivers are DC-coupled, contact 4DSP for other configurations.

#### 4.1.3.2 Front I/O (LVTTL/TTL)

A voltage translator is used for the (LV)TTL signals available on the front panel. The front side is either 3.3V for LVTTL (default) or 5.0V for TTL (build option). These inputs are 5V tolerant when powered with 3.3V. One side of the voltage translator connects to the front I/O signals; the other side connects directly to the FMC connector with levels that operate at VADJ. The direction of each front I/O signal is controlled by the CPLD.

## 4.2 Electrical specifications

The FMC12X uses high-speed LVDS outputs. Revision 1 boards require +2.5V on VADJ power supply (supplied by the carrier card). Revision 2 boards can operate with a VADJ voltage range of 1.65V to 3.3V, but typically VADJ will be 1.8V or 2.5V for LVDS operation.

The voltage on VIO_B pins will be at the same level as VADJ as it is connected directly to VADJ on the FMC12X.

The data converters operate in LVDS mode (clock and data pairs). All other status and control signals, like serial communication busses, operate at LVCMOS level ($V_{OH}$ = VADJ).

### 4.2.1 EEPROM

The FMC12X card carries a 2Kbit EEPROM which is accessible from the carrier card through the $I^2C$ bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01µA when SCL and SDA are kept at 3P3VAUX level. These signals may also be left floating since pull-up resistors are present on the card.

### 4.2.2 JTAG

The CPLD device is included in the JTAG chain accessible from the FMC connection. The user should **NOT** reprogram or erase the CPLD.

### 4.2.3 FMC Connector

The high-pin count connector has four dedicated LVDS clock pairs and can host up to 80 LVDS (data) pairs of which some are defined as clock capable. The 80 pairs are divided into three banks:

- Bank LA with 34 pairs, of which four are clock capable.
- Bank HA with 24 pairs, of which three are clock capable.
- Bank HB with 22 pairs, of which three are clock capable.

The low-pin count connector has only bank LA available and only two of the four dedicated LVDS clock pairs. The following arrangement is used:

- ADC output port A and port B will connect to bank LA.
  (32 data pairs and 2 clock capable pairs on FMC122/FMC125)
  (20 data pairs and 2 clock capable pairs on FMC126)
- ADC output port C will connect to bank HA.
  (16 data pairs and 1 clock capable pairs on FMC122/FMC125)
  (10 data pairs and 1 clock capable pairs on FMC126)
- ADC output port D will connect to bank HB.
  (16 data pairs and 1 clock capable pairs on FMC122/FMC125)
  (10 data pairs and 1 clock capable pairs on FMC126)

The over range signal pairs are connected to bank HA/HB and are therefore not available on carrier boards with a low-pin count connector.

### 4.2.4 Main characteristics

| Analog inputs | |
|---|---|
| **Number of channels** | 4, 2, or 1 (programmable) |
| **Channel resolution** | 8-bit (FMC122/FMC125)<br>10-bit (FMC126) |

| | |
|---|---|
| **Input voltage range** | 0.5Vp-p |
| **Input impedance** | 50Ω AC-coupled |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **Analogue input bandwidth** | 500/600/1500/2000MHz programmable (FMC122/FMC125)<br>1000/3000MHz programmable (FMC126) |
| **Performance (Fin = 406 MHz)** | SFDR = 56 dBc, SNR = 44 dBFS (FMC122/FMC125, 1.25Gsps mode)<br>SFDR = 61 dBc, SNR = 50 dBFS (FMC126, 1.25Gsps mode) |
| **Calibration** | Gain ±18%<br>Offset ±50mV<br>Phase ±14ps |
| **External Clock/Reference input** | |
| **Input level** | -6dBm to +7dBm |
| **Input impedance** | 50Ω AC-coupled |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **Frequency range** | 10 – 100 MHz (reference clock)<br>400 – 2500 MHz (sample clock) |
| **External Clock Output (optional)** | |
| **Output level** | -4dBm to +3dBm |
| **Output waveform** | Square, AC-coupled |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **External Trigger/Sync input** | |
| **Input threshold level** | 1.25V typical (LVTTL level supported) |
| **Input impedance** | 2.5kΩ DC-coupled |
| **Connector type** | SSMC (AEP 7110-1511-000) |
| **Frequency range** | Up to 625 MHz |
| **ADC Output** | |
| **Output data width** | LVDS 1:2, 8x 8-pairs DDR (FMC122/FMC125)<br>LVDS 1:1, 4x 10-pairs DDR (FMC126) |
| **Data Format** | Offset binary |
| **FMC connector type** | HPC (ASP-134488-01) |
| **Sampling Frequency Range** | 200 – 1250 MHz (4-channel mode)<br>400 – 2500 MHz (2-channel mode)<br>800 – 5000 MHz (1-channel mode) |
| **Internal Clock/Reference** | |
| **Format** | LVPECL |
| **Frequency Range** | 100 MHz (reference clock)<br>2500MHz (sample clock, enables full speed sampling in 4-, 2-, and 1-channel mode)<br>Optionally the onboard VCXO clock (2500MHz) can be divided down to allow lower sampling frequencies. Divider factors are 2,3,4,5, and 6. |

**Table 3 : FMC12x daughter card main characteristics**

## 4.3 Analog input channels

The FMC125/FMC126 has four analog inputs which are AC-coupled to the Quad ADC. There is a flexible analog input switch enabling 4- , 2-, and 1-channel mode.

In two channel mode one input connects to either input A or B. The other input connects to either input C or D. In one channel mode the analog signal may be connecter to either one of the four inputs A, B, C, or D.

On the FMC122 a maximum of two analog inputs (A and B) can be sampled simultaneously.

## 4.4 External clock input

The actual sampling clock ($F_S$) can be derived from the external clock input ($F_{EXT}$) as follows:

- 4-channel mode: $F_S = F_{EXT} / 2$ ($F_{S,MAX}$ = 1.25Gsps)
- 2-channel mode: $F_S = F_{EXT}$ ($F_{S,MAX}$ = 2.50Gsps)
- 1-channel mode: $F_S = F_{EXT} \times 2$ ($F_{S,MAX}$ = 5.00Gsps)

## 4.5 External trigger/sync input

The external trigger input can be configured in different ways (build options). The trigger input can be 50Ω terminated accepting most common high-speed signalling standards like single-ended LVPECL. By default, the 50Ω termination is not mounted in order to support LVTTL/LVCMOS and similar input standards. Differential input is also possible using the coax shield as inverted signal. By default, the input is single-ended DC coupled with an impedance of approximately 2.5kΩ. The input threshold is approximately 1.25V.

Optionally, the trigger input can be used as sync input, synchronizing local A/D converters or multiple FMC12x cards.

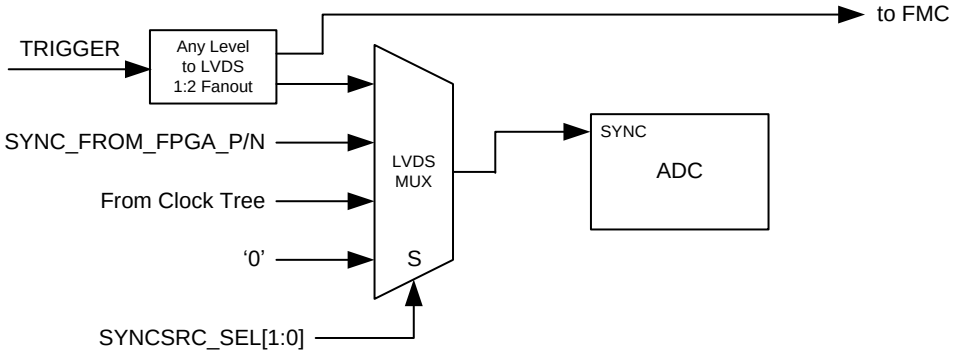


**Figure 6: A/D Synchronization topology**

## 4.6 Clock Tree

The FMC12x offers a clock architecture that combines flexibility and high performance. Components have been chosen in order to minimize jitter and phase noise to reduce degradation of the data conversion performance. The user may choose to use an external or internal sampling clock.

The clock tree has a PLL and clock distribution section. The PLL ensures locking of the internal clock to an external supplied reference. The onboard reference is used if no external reference is present.

A 2500MHz VCO (CRO2500A-LF) is used as internal clock source and can connect to the distribution section instead of the external clock input. The distribution section drives the Quad ADC. One additional clock signal is connected to the FMC connector for test and monitoring purposes.

Note that the LF input on the AD9517 is not connected to the loop filter. It is therefore not possible to use the internal VCO of the AD9517.

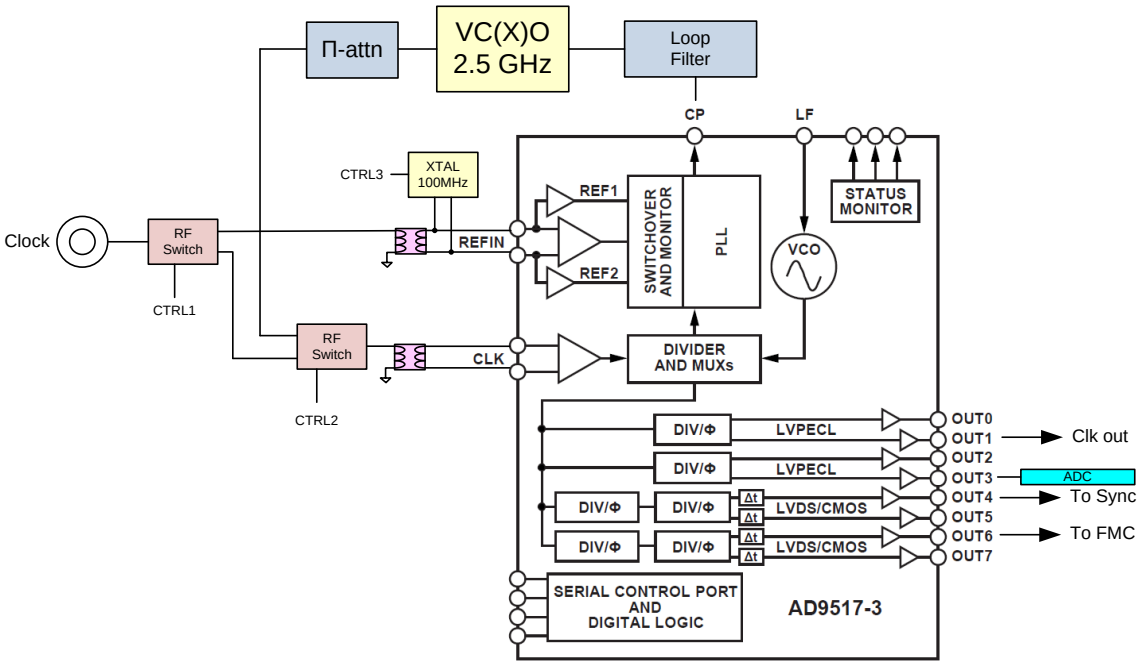


**Figure 7: Clock tree**

### Control

The clock tree contains two RF switches (ADG918) and requires the following control signals (driven from the CPLD):

- CLKSRC_SEL0 connects the external clock input to the reference input of the AD9517 or the 2nd RF switch.
- CLKSRC_SEL1 connect either the onboard VCXO or the external clock to the clock input of the AD9517. This signal also controls the VCXO power supply[1].
- CLKSRC_SEL2 enables/disables the onboard reference oscillator.

## 4.7 Multi-Gigabit Transceivers (optional)

The FMC connector hosts 10 MGT pairs (10 Tx and 10 Rx pairs). These are connected to two 38-pins MICTOR headers in an arrangement that supports different interconnect topologies.

[1] The VCXO should be powered down to avoid interference with the external clock when external clock is used.

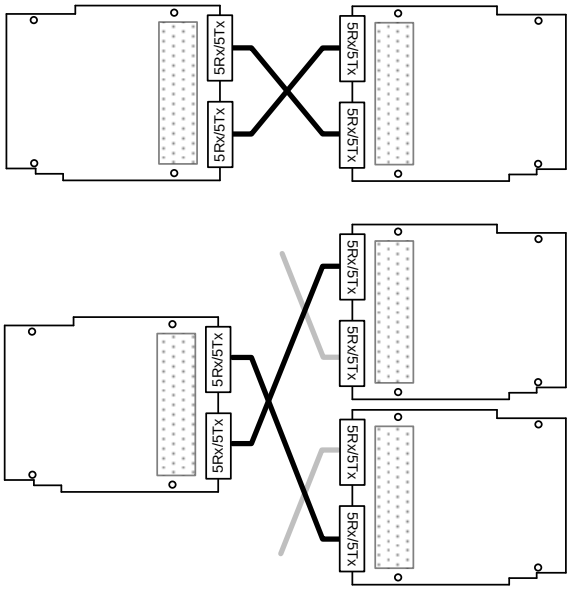


**Figure 8: MGT interconnect topologies**

**TOP VIEW**

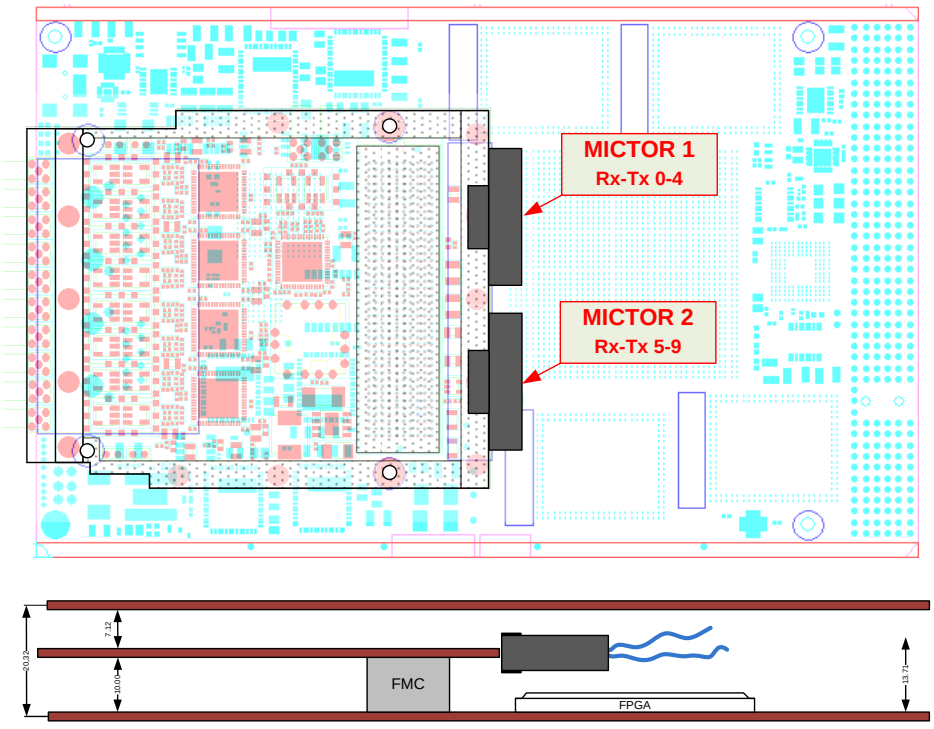


**Figure 9: 4DSP CPCI board stack (slot-to-slot)**

| MICTOR 1 | | | | |
|---|---|---|---|---|
| Pin | Signal | Midplate | Signal | Pin |
| 1 | GND | GND | GND | 2 |
| 3 | TX0_P* | GND | RX0_P* | 4 |
| 5 | TX0_N* | GND | RX0_N* | 6 |
| 7 | GND | GND | GND | 8 |
| 9 | TX1_P* | GND | RX1_P* | 10 |
| 11 | TX1_N* | GND | RX1_N* | 12 |
| 13 | GND | GND | GND | 14 |
| 15 | TX2_P* | GND | RX2_P* | 16 |
| 17 | TX2_N* | GND | RX2_N* | 18 |
| 19 | GND | GND | GND | 20 |
| 21 | TX3_P* | GND | RX3_P* | 22 |
| 23 | TX3_N* | GND | RX3_N* | 24 |
| 25 | GND | GND | GND | 26 |
| 27 | TX4_P | GND | RX4_P | 28 |
| 29 | TX4_N | GND | RX4_N | 30 |
| 31 | GND | GND | GND | 32 |
| 33 | IO0 | GND | | 34 |
| 35 | IO1 | GND | | 36 |
| 37 | GND | GND | GND | 38 |

| MICTOR 2 | | | | |
|---|---|---|---|---|
| Pin | Signal | Midplate | Signal | Pin |
| 1 | GND | GND | GND | 2 |
| 3 | RX9_P | GND | TX9_P | 4 |
| 5 | RX9_N | GND | TX9_N | 6 |
| 7 | GND | GND | GND | 8 |
| 9 | RX8_P | GND | TX8_P | 10 |
| 11 | RX8_N | GND | TX8_N | 12 |
| 13 | GND | GND | GND | 14 |
| 15 | RX7_P | GND | TX7_P | 16 |
| 17 | RX7_N | GND | TX7_N | 18 |
| 19 | GND | GND | GND | 20 |
| 21 | RX6_P | GND | TX6_P | 22 |
| 23 | RX6_N | GND | TX6_N | 24 |
| 25 | GND | GND | GND | 26 |
| 27 | RX5_P | GND | TX5_P | 28 |
| 29 | RX5_N | GND | TX5_N | 30 |
| 31 | GND | GND | GND | 32 |
| 33 | IO2 | GND | | 34 |
| 35 | IO3 | GND | | 36 |
| 37 | GND | GND | GND | 38 |

**Table 4. MGT connector pinout[2]**

A low phase noise 125MHz XTAL is used as reference clock. A 1:2 LVDS fan-out buffer is used to feed to reference clock to both connections on the FMC connector.

The pairs marked with * connects to either the MICTOR header or the HDMI connector. The assembly is determined with 0Ω resistors. A maximum of four pairs can connect to the HDMI connector. Contact 4DSP for custom configurations.

**NOTE: These connectors will breach the FMC specification and are therefore a build option. Please contact the factory for more information.**

**N.B.** These connectors are not available on the FMC12X revision 2.

## 4.8 Power supply

Power is supplied to the FMC12x card through the FMC connector. The pin current rating is 2.7A, but the overall maximum as specified by the FMC standard is limited according to Table 5.

[2] Signals IO[0:3] connects to the CPLD and has no defined function yet.

| Voltage | # pins | Max Amps | Max Watt |
|---|---|---|---|
| +3.3V | 4 | 3 A | 10 W |
| +12V | 2 | 1 A | 12 W |
| VADJ (+2.5V) | 4 | 4 A | 10 W |
| VIO_B (+2.5V) | 2 | 1.15 A | 2.3 W |

**Table 5: FMC standard power specification**

The power provided by the carrier card can be very noisy. Special care is taken with the power supply generation on the FMC12x card to minimize the effect of power supply noise on clock generation and data conversion.

Clean analog supply (+3.3V) is derived from +12V in two steps for maximum efficiency. The first step uses a highly efficient switched regulator to generate a +3.8V power rail. From this power rail, the analog supply is derived with a low dropout, low noise, high PSRR, linear regulator. There is additional noise filtering at several stages in the power supply.

The regulators have sufficient copper area to dissipate the heat in combination with proper airflow (see section 6.3 Cooling)

| Power plane | Typical | Maximum |
|---|---|---|
| VADJ | 665mA | 685mA |
| 3P3V | 50mA | 95mA |
| 12P0V | 900mA | 920mA |
| 3P3VAUX (Operating)<br>3P3VAUX (Standby) | 0.1 mA<br>0.01 µA | 3 mA<br>1 µA |

**Table 6a: Typical/Maximum current drawn from FMC12X revision 1**

| Power plane | Typical | Maximum |
|---|---|---|
| VADJ | 25mA | 25mA |
| 3P3V | 540mA | 610mA |
| 12P0V | 900mA | 920mA |
| 3P3VAUX (Operating)<br>3P3VAUX (Standby) | 0.1 mA<br>0.01 µA | 3 mA<br>1 µA |

**Table 6b: Typical/Maximum current drawn from FMC12X revision 2**

The total power consumption: 13W

### 4.9 DIP-Switches

The DIP-Switches should be in the state as indicated in the following table. Any other configuration might affect the analog conversion performance.

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| **FMC122** | OFF | OFF | ON | OFF |
| **FMC125** | OFF | OFF | ON | OFF |
| **FMC126** | ON | ON | OFF | OFF |

**Table 6: Default DIP-Switch state**

## 5 Controlling the FMC12x

The FMC12x is fully controlled from the carrier hardware through a single I²C communication bus. Three devices are connected, refer to Table 7. The device addresses depend on the global address pins defined by the FMC standard (GA0, GA1). Note that the ADT7411 uses only GA0.

| Device | Description | I²C Address |
|---|---|---|
| 24LC02B | 2K I²C Serial EEPROM | 1 0 1 0 0 GA1 GA0 |
| SC18IS602B | I²C-bus to SPI bridge | 0 1 0 1 0 GA1 GA0 |
| ADT7411 | Digital Temperature Sensor and A/D | 1 0 0 1 0 GA0 GA0 |

**Table 7: I²C devices**

The I²C-bus to SPI bridge (SC18IS602B) supports four SPI slaves. The following slaves are assigned:

SS0: AD9517
SS1: A/D device
SS2: -
SS3: CPLD

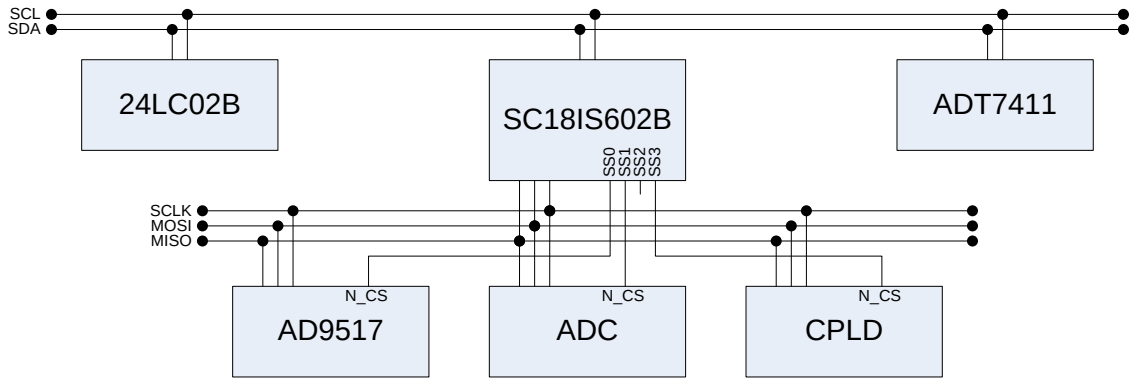


**Figure 10: I²C / SPI architecture**

The CPLD has the following tasks:

- Select clock source based on a SPI command (CLKSRC_SEL)
- Select sync source based on a SPI command (SYNCSRC_SEL)
- Generate SPI reset for AD9517 (CLK_N_RESET) and A/D (ADC_N_RESET)
- Control the direction of the front I/O transceivers (FRONT_IO_DIR)
- Control the FAN header power (FAN_N_EN)
- Collect local status signals and store them in a register which can be accessed from the carrier hardware
- Drive a LED according to the level of the status signals

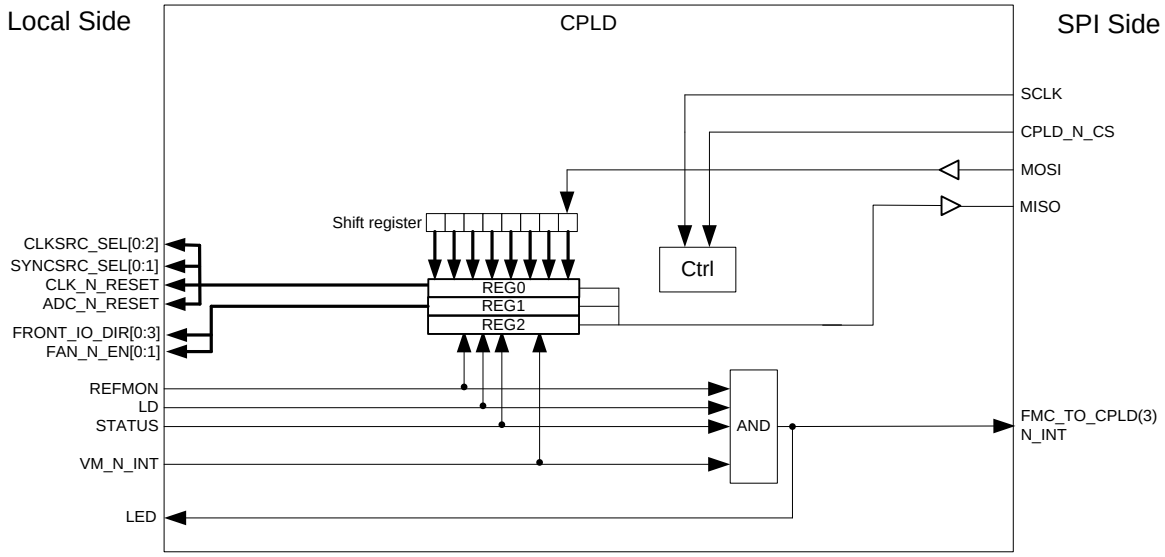


**Figure 11: CPLD architecture**

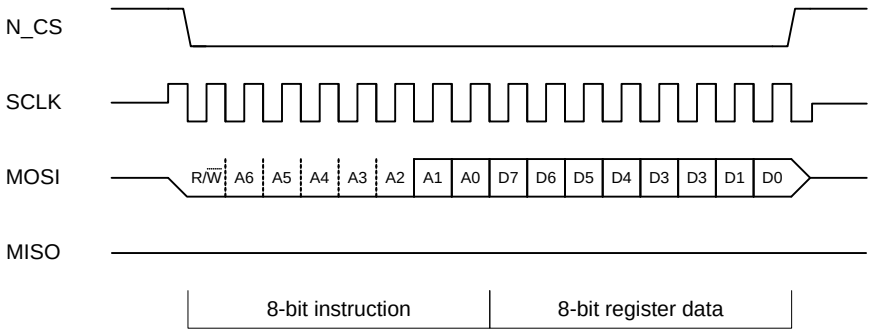


**Figure 12: Write instruction to CPLD registers A1:A0**

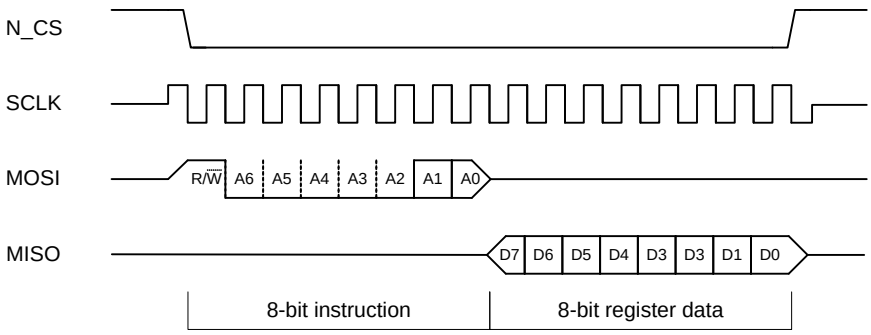


**Figure 13: Read instruction to CPLD registers A1:A0**

# 6 Environment

## 6.1 Temperature

Operating temperature

- 0˚C to +70˚C (Commercial)

Storage temperature:

- -40˚C to +120˚C

## 6.2 Monitoring

The onboard monitoring may be used to monitor the voltage on the different power rails as well as the temperature of the Quad ADC and the clock tree.

It is recommended that the carrier card and/or host software uses the power-down features of the Quad ADC and the clock tree if the temperature is too high. Normal operations can resume once the temperature is within the operating conditions boundaries.

| Parameter: | Device 1 | Formula |
|---|---|---|
| On-chip temperature | ADT7411 Die Temperature | |
| On-chip AIN0 ($V_{DD}$) | +3.3V | |
| External temperature | ADC Die Temperature | |
| External AIN3 | VADJ | AIN3 |
| External AIN4 | +2.5V Analog | AIN4 |
| External AIN5 | +3.3V Digital | AIN5 * 2 |
| External AIN6 | +3.3V Analog | AIN6 * 2 |
| External AIN7 | VCP | AIN7 * 2 |
| External AIN8 | +1.8V Digital | AIN8 |

**Table 8: Temperature and voltage parameters**

## 6.3 Cooling

Two different types of cooling are available for the FMC12x.

### 6.3.1 Convection cooling

The air flow provided by the fans of the chassis the FMC12x is enclosed in will dissipate the heat generated by the onboard components. A minimum airflow of 300 LFM is recommended.

Optionally, a low profile heat sink/fan can be glued on top of the Quad ADC. The card has a fan power connection that can be switch on and off under carrier card control. The FAN power voltage is 3.3V and can be switched on and off through a CPLD register (refer to Table 14).

For standalone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC and ensure that the temperature of the devices is within the allowed

range. 4DSP's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

### 6.3.2 Conduction cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions the junction temperature of power consuming devices will exceed the operating conditions recommended by the device manufacturers (mostly +85°C).

The FMC12x is designed for maximum heat transfer to conduction-cooled ribs. A customized cooling frame that connects directly to the surface of the Quad ADC is allowed (contact 4DSP for detailed mechanical information). This conduction-cooling mechanism should be applied in combination with proper chassis air flow.

# 7 Safety

This module presents no hazard to the user.

# 8 EMC

This module is designed to operate within an enclosed host system built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

# 9 Warranty

| | *Hardware* | *Software/Firmware* |
|---|---|---|
| Basic Warranty (included) | 1 Year from Date of Shipment | 90 Days from Date of Shipment |
| Extended Warranty (optional) | 2 Years from Date of Shipment | 1 Year from Date of Shipment |

# Appendix A LPC pin-out FMC122

| AV57.1 | LPC Pin | FMC122 Signal | AV57.1 | LPC Pin | FMC122 Signal | AV57.1 | LPC Pin | FMC122 Signal |
|---|---|---|---|---|---|---|---|---|
| CLK0_M2C_N | H5 | CLK_TO_FPGA_N | | | | GBTCLK0_M2C_N | D5 | GBTCLK0_N |
| CLK0_M2C_P | H4 | CLK_TO_FPGA_P | | | | GBTCLK0_M2C_P | D4 | GBTCLK0_P |
| CLK1_M2C_N | G3 | TRIGGER_TO_FPGA_N | | | | | | |
| CLK1_M2C_P | G2 | TRIGGER_TO_FPGA_P | | | | | | |
| LA00_N_CC | G7 | ADR_N | LA17_N_CC | D21 | BDR_N | DP0_C2M_N | C3 | DP_C2M_N<0> |
| LA00_P_CC | G6 | ADR_P | LA17_P_CC | D20 | BDR_P | DP0_C2M_P | C2 | DP_C2M_P<0> |
| LA01_N_CC | D9 | ALD_N<0> | LA18_N_CC | C23 | BLD_N<0> | DP0_M2C_N | C7 | DP_M2C_N<0> |
| LA01_P_CC | D8 | ALD_P<0> | LA18_P_CC | C22 | BLD_P<0> | DP0_M2C_P | C6 | DP_M2C_P<0> |
| LA02_N | H8 | AHD_N<0> | LA19_N | H23 | BHD_N<0> | | | |
| LA02_P | H7 | AHD _P<0> | LA19_P | H22 | BHD _P<0> | | | |
| LA03_N | G10 | ALD_N<1> | LA20_N | G22 | BLD_N<1> | | | |
| LA03_P | G9 | ALD_P<1> | LA20_P | G21 | BLD_P<1> | | | |
| LA04_N | H11 | AHD_N<1> | LA21_N | H26 | BHD_N<1> | | | |
| LA04_P | H10 | AHD_P<1> | LA21_P | H25 | BHD_P<1> | | | |
| LA05_N | D12 | ALD_N<2> | LA22_N | G25 | BLD_N<2> | | | |
| LA05_P | D11 | ALD_P<2> | LA22_P | G24 | BLD_P<2> | | | |
| LA06_N | C11 | AHD_N<2> | LA23_N | D24 | BHD_N<2> | | | |
| LA06_P | C10 | AHD_P<2> | LA23_P | D23 | BHD_P<2> | | | |
| LA07_N | H14 | ALD_N<3> | LA24_N | H29 | BLD_N<3> | | | |
| LA07_P | H13 | ALD_P<3> | LA24_P | H28 | BLD_P<3> | | | |
| LA08_N | G13 | AHD_N<3> | LA25_N | G28 | BHD_N<3> | | | |
| LA08_P | G12 | AHD_P<3> | LA25_P | G27 | BHD_P<3> | | | |
| LA09_N | D15 | ALD_N<6> | LA26_N | D27 | BLD_N<6> | | | |
| LA09_P | D14 | ALD_P<6> | LA26_P | D26 | BLD_P<6> | | | |
| LA10_N | C15 | ALD_N<7> | LA27_N | C27 | BLD_N<7> | | | |
| LA10_P | C14 | ALD_P<7> | LA27_P | C26 | BLD_P<7> | | | |
| LA11_N | H17 | ALD_N<4> | LA28_N | H32 | BLD_N<4> | | | |
| LA11_P | H16 | ALD_P<4> | LA28_P | H31 | BLD_P<4> | | | |
| LA12_N | G16 | AHD_N<4> | LA29_N | G31 | BHD_N<4> | | | |
| LA12_P | G15 | AHD_P<4> | LA29_P | G30 | BHD_P<4> | | | |
| LA13_N | D18 | ALD_N<5> | LA30_N | H35 | BLD_N<5> | | | |
| LA13_P | D17 | ALD_P<5> | LA30_P | H34 | BLD_P<5> | | | |
| LA14_N | C19 | AHD_N<5> | LA31_N | G34 | BHD_N<5> | | | |
| LA14_P | C18 | AHD_P<5> | LA31_P | G33 | BHD_P<5> | | | |
| LA15_N | H20 | AHD_N<6> | LA32_N | H38 | BHD_N<6> | | | |
| LA15_P | H19 | AHD_P<6> | LA32_P | H37 | BHD_P<6> | | | |
| LA16_N | G19 | AHD_N<7> | LA33_N | G37 | BHD_N<7> | SCL | C30 | I2C_SCL |
| LA16_P | G18 | AHD_P<7> | LA33_P | G36 | BHD_P<7> | SDA | C31 | I2C_SDA |

**Table 9: FMC122 signal description**

| Signal | Group | Direction | I/O Standard | Description |
|---|---|---|---|---|
| ADR_N<br>ADR_P | A/D A | Output | LVDS | Digital data clock from ADC. The ADC can operate in mux mode, using data port L(ow) and data port H(igh) |
| ALD_N<7..0><br>ALD_P<7..0> | A/D A | Output | LVDS | Data port L(ow), data is valid on both edges of the clock (DDR) |
| AHD_N<7..0><br>AHD_P<7..0> | A/D A | Output | LVDS | Data port H(igh), data is valid on both edges of the clock (DDR) |
| BDR_N<br>BDR_P | A/D B | Output | LVDS | Digital data clock from ADC. The ADC can operate in mux mode, using data port L(ow) and data port H(igh) |
| BLD_N<7..0><br>BLD_P<7..0> | A/D B | Output | LVDS | Data port L(ow), data is valid on both edges of the clock (DDR) |
| BHD_N<7..0><br>BHD_P<7..0> | A/D B | Output | LVDS | Data port H(igh), data is valid on both edges of the clock (DDR) |
| CLK_TO_FPGA_N<br>CLK_TO_FPGA_P | MONITOR | Output | LVDS | Spare clock signal from the clock tree. Can be used to monitor onboard/external clock. |
| TRIGGER_TO_FPGA_N<br>TRIGGER_TO_FPGA_P | I/O | Output | LVDS | Representation of the signal connected to the external trigger input. |
| I2C_SCL | CONTROL | Input | LVTTL 3.3V | I2C Clock. The I2C bus is the main control bus. |
| I2C_SDA | CONTROL | Bidir | LVTTL 3.3V | I2C Data. The I2C bus is the main control bus. |
| DP_M2C_P/N0 | O | Output | CML/ECL | Gigabit transceiver from HDMI connector |

# Appendix B HPC pin-out FMC125/FMC122

| AV57.1 | HPC Pin | FMC125 Signal | AV57.1 | HPC Pin | FMC125 Signal | AV57.1 | HPC Pin | FMC125 Signal |
|---|---|---|---|---|---|---|---|---|
| CLK0_M2C_N | H5 | CLK_TO_FPGA_N | CLK2_BIDIR_N | K5 | SYNC_FROM_FPGA_N | GBTCLK0_M2C_N | D5 | GBTCLK0_N |
| CLK0_M2C_P | H4 | CLK_TO_FPGA_P | CLK2_BIDIR_P | K4 | SYNC_FROM_FPGA_P | GBTCLK0_M2C_P | D4 | GBTCLK0_P |
| CLK1_M2C_N | G3 | TRIGGER_TO_FPGA_N | CLK3_BIDIR_N | J3 | N.C. | GBTCLK1_M2C_N | B21 | GBTCLK1_N |
| CLK1_M2C_P | G2 | TRIGGER_TO_FPGA_P | CLK3_BIDIR_P | J2 | N.C. | GBTCLK1_M2C_P | B20 | GBTCLK1_P |
| LA00_N_CC | G7 | ADR_N | HA00_N_CC | F5 | CDR_N | HB00_N_CC | K26 | DDR_N |
| LA00_P_CC | G6 | ADR_P | HA00_P_CC | F4 | CDR_P | HB00_P_CC | K25 | DDR_P |
| LA01_N_CC | D9 | ALD_N<0> | HA01_N_CC | E3 | CLD_N<0> | HB01_N | J25 | DLD_N<0> |
| LA01_P_CC | D8 | ALD_P<0> | HA01_P_CC | E2 | CLD_P<0> | HB01_P | J24 | DLD_P<0> |
| LA02_N | H8 | AHD_N<0> | HA02_N | K8 | CHD_N<0> | HB02_N | F23 | DHD_N<0> |
| LA02_P | H7 | AHD _P<0> | HA02_P | K7 | CHD _P<0> | HB02_P | F22 | DHD _P<0> |
| LA03_N | G10 | ALD_N<1> | HA03_N | J7 | CLD_N<1> | HB03_N | E22 | DLD_N<1> |
| LA03_P | G9 | ALD_P<1> | HA03_P | J6 | CLD_P<1> | HB03_P | E21 | DLD_P<1> |
| LA04_N | H11 | AHD_N<1> | HA04_N | F8 | CHD_N<1> | HB04_N | F26 | DHD_N<1> |
| LA04_P | H10 | AHD_P<1> | HA04_P | F7 | CHD_P<1> | HB04_P | F25 | DHD_P<1> |
| LA05_N | D12 | ALD_N<2> | HA05_N | E7 | CLD_N<2> | HB05_N | E25 | DLD_N<2> |
| LA05_P | D11 | ALD_P<2> | HA05_P | E6 | CLD_P<2> | HB05_P | E24 | DLD_P<2> |
| LA06_N | C11 | AHD_N<2> | HA06_N | K11 | CHD_N<2> | HB06_N_CC | K29 | DHD_N<2> |
| LA06_P | C10 | AHD_P<2> | HA06_P | K10 | CHD_P<2> | HB06_P_CC | K28 | DHD_P<2> |
| LA07_N | H14 | ALD_N<3> | HA07_N | J10 | CLD_N<3> | HB07_N | J28 | DLD_N<3> |
| LA07_P | H13 | ALD_P<3> | HA07_P | J9 | CLD_P<3> | HB07_P | J27 | DLD_P<3> |
| LA08_N | G13 | AHD_N<3> | HA08_N | F11 | CHD_N<3> | HB08_N | F29 | DHD_N<3> |
| LA08_P | G12 | AHD_P<3> | HA08_P | F10 | CHD_P<3> | HB08_P | F28 | DHD_P<3> |
| LA09_N | D15 | ALD_N<6> | HA09_N | E10 | CLD_N<6> | HB09_N | E28 | DLD_N<6> |
| LA09_P | D14 | ALD_P<6> | HA09_P | E9 | CLD_P<6> | HB09_P | E27 | DLD_P<6> |
| LA10_N | C15 | ALD_N<7> | HA10_N | K14 | CLD_N<7> | HB10_N | K32 | DLD_N<7> |
| LA10_P | C14 | ALD_P<7> | HA10_P | K13 | CLD_P<7> | HB10_P | K31 | DLD_P<7> |
| LA11_N | H17 | ALD_N<4> | HA11_N | J13 | CLD_N<4> | HB11_N | J31 | DLD_N<4> |
| LA11_P | H16 | ALD_P<4> | HA11_P | J12 | CLD_P<4> | HB11_P | J30 | DLD_P<4> |
| LA12_N | G16 | AHD_N<4> | HA12_N | F14 | CHD_N<4> | HB12_N | F32 | DHD_N<4> |
| LA12_P | G15 | AHD_P<4> | HA12_P | F13 | CHD_P<4> | HB12_P | F31 | DHD_P<4> |
| LA13_N | D18 | ALD_N<5> | HA13_N | E13 | CLD_N<5> | HB13_N | E31 | DLD_N<5> |
| LA13_P | D17 | ALD_P<5> | HA13_P | E12 | CLD_P<5> | HB13_P | E30 | DLD_P<5> |
| LA14_N | C19 | AHD_N<5> | HA14_N | J16 | CHD_N<5> | HB14_N | K35 | DHD_N<5> |
| LA14_P | C18 | AHD_P<5> | HA14_P | J15 | CHD_P<5> | HB14_P | K34 | DHD_P<5> |
| LA15_N | H20 | AHD_N<6> | HA15_N | F17 | CHD_N<6> | HB15_N | J34 | DHD_N<6> |
| LA15_P | H19 | AHD_P<6> | HA15_P | F16 | CHD_P<6> | HB15_P | J33 | DHD_P<6> |
| LA16_N | G19 | AHD_N<7> | HA16_N | E16 | CHD_N<7> | HB16_N | F35 | DHD_N<7> |
| LA16_P | G18 | AHD_P<7> | HA16_P | E15 | CHD_P<7> | HB16_P | F34 | DHD_P<7> |
| LA17_N_CC | D21 | BDR_N | HA17_N_CC | K17 | CLOR_N | HB17_N_CC | K38 | DLOR_N |
| LA17_P_CC | D20 | BDR_P | HA17_P_CC | K16 | CLOR_P | HB17_P_CC | K37 | DLOR_P |
| LA18_N_CC | C23 | BLD_N<0> | HA18_N | J19 | CHOR_N | HB18_N | J37 | DHOR_N |
| LA18_P_CC | C22 | BLD_P<0> | HA18_P | J18 | CHOR_P | HB18_P | J36 | DHOR_P |
| LA19_N | H23 | BHD_N<0> | HA19_N | F20 | ALOR_N | HB19_N | E34 | FMC_TO_CPLD<3> |
| LA19_P | H22 | BHD _P<0> | HA19_P | F19 | ALOR_P | HB19_P | E33 | FMC_TO_CPLD<2> |
| LA20_N | G22 | BLD_N<1> | HA20_N | E19 | AHOR_N | HB20_N | F38 | FRONT_IO_FMC<1> |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LA20_P | G21 | BLD_P<1> | HA20_P | E18 | AHOR_P | HB20_P | F37 | FRONT_IO_FMC<0> |
| LA21_N | H26 | BHD_N<1> | HA21_N | K20 | BLOR_N | HB21_N | E37 | FRONT_IO_FMC<3> |
| LA21_P | H25 | BHD_P<1> | HA21_P | K19 | BLOR_P | HB21_P | E36 | FRONT_IO_FMC<2> |
| LA22_N | G25 | BLD_N<2> | HA22_N | J22 | BHOR_N | | | |
| LA22_P | G24 | BLD_P<2> | HA22_P | J21 | BHOR_P | | | |
| LA23_N | D24 | BHD_N<2> | HA23_N | K23 | FMC_TO_CPLD<1> | SCL | C30 | I2C_SCL |
| LA23_P | D23 | BHD_P<2> | HA23_P | K22 | FMC_TO_CPLD<0> | SDA | C31 | I2C_SDA |
| LA24_N | H29 | BLD_N<3> | DP0_C2M_N | C3 | DP_C2M_N<0> | DP0_M2C_N | C7 | DP_M2C_N<0> |
| LA24_P | H28 | BLD_P<3> | DP0_C2M_P | C2 | DP_C2M_P<0> | DP0_M2C_P | C6 | DP_M2C_P<0> |
| LA25_N | G28 | BHD_N<3> | DP1_C2M_N | A23 | DP_C2M_N<1> | DP1_M2C_N | A3 | DP_M2C_N<1> |
| LA25_P | G27 | BHD_P<3> | DP1_C2M_P | A22 | DP_C2M_P<1> | DP1_M2C_P | A2 | DP_M2C_P<1> |
| LA26_N | D27 | BLD_N<6> | DP2_C2M_N | A27 | DP_C2M_N<2> | DP2_M2C_N | A7 | DP_M2C_N<2> |
| LA26_P | D26 | BLD_P<6> | DP2_C2M_P | A26 | DP_C2M_P<2> | DP2_M2C_P | A6 | DP_M2C_P<2> |
| LA27_N | C27 | BLD_N<7> | DP3_C2M_N | A31 | DP_C2M_N<3> | DP3_M2C_N | A11 | DP_M2C_N<3> |
| LA27_P | C26 | BLD_P<7> | DP3_C2M_P | A30 | DP_C2M_P<3> | DP3_M2C_P | A10 | DP_M2C_P<3> |
| LA28_N | H32 | BLD_N<4> | DP4_C2M_N | A35 | DP_C2M_N<4> | DP4_M2C_N | A15 | DP_M2C_N<4> |
| LA28_P | H31 | BLD_P<4> | DP4_C2M_P | A34 | DP_C2M_P<4> | DP4_M2C_P | A14 | DP_M2C_P<4> |
| LA29_N | G31 | BHD_N<4> | DP5_C2M_N | A39 | DP_C2M_N<5> | DP5_M2C_N | A19 | DP_M2C_N<5> |
| LA29_P | G30 | BHD_P<4> | DP5_C2M_P | A38 | DP_C2M_P<5> | DP5_M2C_P | A18 | DP_M2C_P<5> |
| LA30_N | H35 | BLD_N<5> | DP6_C2M_N | B37 | DP_C2M_N<6> | DP6_M2C_N | B17 | DP_M2C_N<6> |
| LA30_P | H34 | BLD_P<5> | DP6_C2M_P | B36 | DP_C2M_P<6> | DP6_M2C_P | B16 | DP_M2C_P<6> |
| LA31_N | G34 | BHD_N<5> | DP7_C2M_N | B33 | DP_C2M_N<7> | DP7_M2C_N | B13 | DP_M2C_N<7> |
| LA31_P | G33 | BHD_P<5> | DP7_C2M_P | B32 | DP_C2M_P<7> | DP7_M2C_P | B12 | DP_M2C_P<7> |
| LA32_N | H38 | BHD_N<6> | DP8_C2M_N | B29 | DP_C2M_N<8> | DP8_M2C_N | B9 | DP_M2C_N<8> |
| LA32_P | H37 | BHD_P<6> | DP8_C2M_P | B28 | DP_C2M_P<8> | DP8_M2C_P | B8 | DP_M2C_P<8> |
| LA33_N | G37 | BHD_N<7> | DP9_C2M_N | B25 | DP_C2M_N<9> | DP9_M2C_N | B5 | DP_M2C_N<9> |
| LA33_P | G36 | BHD_P<7> | DP9_C2M_P | B24 | DP_C2M_P<9> | DP9_M2C_P | B4 | DP_M2C_P<9> |

**Table 10: FMC125/FMC122 signal description**

| Signal | Group | Direction | I/O Standard | Description |
|---|---|---|---|---|
| ADR_N<br>ADR_P | A/D A | Output | LVDS | Digital data clock from ADC. The ADC can operate in mux mode, using data port L(ow) and data port H(igh) |
| ALD_N<7..0><br>ALD_P<7..0> | A/D A | Output | LVDS | Data port L(ow), data is valid on both edges of the clock (DDR) |
| ALOR_N<br>ALOR_P | A/D A | Output | LVDS | Over-range bit synchronous to the samples present on port L(ow). |
| AHD_N<7..0><br>AHD_P<7..0> | A/D A | Output | LVDS | Data port H(igh), data is valid on both edges of the clock (DDR) |
| AHOR_N<br>AHOR_P | A/D A | Output | LVDS | Over-range bit synchronous to the |

| | | | | |
|---|---|---|---|---|
| | | | | samples present on port H(igh). |
| BDR_N<br>BDR_P | A/D B | Output | LVDS | Digital data clock from ADC. The ADC can operate in mux mode, using data port L(ow) and data port H(igh) |
| BLD_N<7..0><br>BLD_P<7..0> | A/D B | Output | LVDS | Data port L(ow), data is valid on both edges of the clock (DDR) |
| BLOR_N<br>BLOR_P | A/D B | Output | LVDS | Over-range bit synchronous to the samples present on port L(ow). |
| BHD_N<7..0><br>BHD_P<7..0> | A/D B | Output | LVDS | Data port H(igh), data is valid on both edges of the clock (DDR) |
| BHOR_N<br>BHOR_P | A/D B | Output | LVDS | Over-range bit synchronous to the samples present on port H(igh). |
| CDR_N<br>CDR_P | A/D C | Output | LVDS | Digital data clock from ADC. The ADC can operate in mux mode, using data port L(ow) and data port H(igh) |
| CLD_N<7..0><br>CLD_P<7..0> | A/D C | Output | LVDS | Data port L(ow), data is valid on both edges of the clock (DDR) |
| CLOR_N<br>CLOR_P | A/D C | Output | LVDS | Over-range bit synchronous to the samples present on port L(ow). |
| CHD_N<7..0><br>CHD_P<7..0> | A/D C | Output | LVDS | Data port H(igh), data is valid on both edges of the clock (DDR) |
| CHOR_N<br>CHOR_P | A/D C | Output | LVDS | Over-range bit synchronous to the samples present on port H(igh). |
| DDR_N<br>DDR_P | A/D D | Output | LVDS | Digital data clock from ADC. The ADC can operate in mux mode, using data port L(ow) and data port H(igh) |
| DLD_N<7..0><br>DLD_P<7..0> | A/D D | Output | LVDS | Data port L(ow), data is valid on both edges of the clock (DDR) |
| DLOR_N<br>DLOR_P | A/D D | Output | LVDS | Over-range bit synchronous to the |

| | | | | |
|---|---|---|---|---|
| | | | | samples present on port L(ow). |
| DHD_N<7..0><br>DHD_P<7..0> | A/D D | Output | LVDS | Data port H(igh), data is valid on both edges of the clock (DDR) |
| DHOR_N<br>DHOR_P | A/D D | Output | LVDS | Over-range bit synchronous to the samples present on port H(igh). |
| CLK_TO_FPGA_N<br>CLK_TO_FPGA_P | MONITOR | Output | LVDS | Spare clock signal from the clock tree. Can be used to monitor onboard/external clock. |
| TRIGGER_TO_FPGA_N<br>TRIGGER_TO_FPGA_P | I/O | Output | LVDS | Representation of the signal connected to the external trigger input. |
| FRONT_IO<3..0> | I/O | Bidir | CMOS VADJ | Connected to the transceivers on the HDMI connector (Table 2). The direction of the transceivers is controlled through a CPLD register. |
| DP_M2C_P/N<1..0> | O | Output | CML/ECL | Gigabit transceiver from HDMI connector |
| DP_C2M_P/N<3..2> | I | Input | CML/ECL | Gigabit transceiver to HDMI connector |
| SYNC_FROM_FPGA_N<br>SYNC_FROM_FPGA_P | CONTROL | Input | LVDS | Signal used to apply a sync pulse to both ADC in order to align the digital outputs on sample basis. |
| FMC_TO_CPLD<3..0> | CONTROL | Bidir | CMOS VADJ | Reserved. |
| I2C_SCL | CONTROL | Input | LVTTL 3.3V | I2C Clock. The I2C bus is the main control bus. |
| I2C_SDA | CONTROL | Bidir | LVTTL 3.3V | I2C Data. The I2C bus is the main control bus. |

# Appendix C HPC pin-out FMC126

| AV57.1 | HPC Pin | FMC126 Signal | AV57.1 | HPC Pin | FMC126 Signal | AV57.1 | HPC Pin | FMC126 Signal |
|---|---|---|---|---|---|---|---|---|
| CLK0_M2C_N | H5 | CLK_TO_FPGA_N | CLK2_BIDIR_N | K5 | SYNC_FROM_FPGA_N | GBTCLK0_M2C_N | D5 | GBTCLK0_N |
| CLK0_M2C_P | H4 | CLK_TO_FPGA_P | CLK2_BIDIR_P | K4 | SYNC_FROM_FPGA_P | GBTCLK0_M2C_P | D4 | GBTCLK0_P |
| CLK1_M2C_N | G3 | TRIGGER_TO_FPGA_N | CLK3_BIDIR_N | J3 | N.C. | GBTCLK1_M2C_N | B21 | GBTCLK1_N |
| CLK1_M2C_P | G2 | TRIGGER_TO_FPGA_P | CLK3_BIDIR_P | J2 | N.C. | GBTCLK1_M2C_P | B20 | GBTCLK1_P |
| LA00_N_CC | G7 | ADR_N | HA00_N_CC | F5 | CDR_N | HB00_N_CC | K26 | DDR_N |
| LA00_P_CC | G6 | ADR_P | HA00_P_CC | F4 | CDR_P | HB00_P_CC | K25 | DDR_P |
| LA01_N_CC | D9 | AD_N<0> | HA01_N_CC | E3 | CD_N<0> | HB01_N | J25 | DD_N<0> |
| LA01_P_CC | D8 | AD_P<0> | HA01_P_CC | E2 | CD_P<0> | HB01_P | J24 | DD_P<0> |
| LA02_N | H8 | AD_N<1> | HA02_N | K8 | CD_N<1> | HB02_N | F23 | DD_N<1> |
| LA02_P | H7 | AD _P<1> | HA02_P | K7 | CD _P<1> | HB02_P | F22 | DD _P<1> |
| LA03_N | G10 | AD_N<2> | HA03_N | J7 | CD_N<2> | HB03_N | E22 | DD_N<2> |
| LA03_P | G9 | AD_P<2> | HA03_P | J6 | CD_P<2> | HB03_P | E21 | DD_P<2> |
| LA04_N | H11 | AD_N<3> | HA04_N | F8 | CD_N<3> | HB04_N | F26 | DD_N<3> |
| LA04_P | H10 | AD_P<3> | HA04_P | F7 | CD_P<3> | HB04_P | F25 | DD_P<3> |
| LA05_N | D12 | AD_N<4> | HA05_N | E7 | CD_N<4> | HB05_N | E25 | DD_N<4> |
| LA05_P | D11 | AD_P<4> | HA05_P | E6 | CD_P<4> | HB05_P | E24 | DD_P<4> |
| LA06_N | C11 | AD_N<5> | HA06_N | K11 | CD_N<5> | HB06_N_CC | K29 | DD_N<5> |
| LA06_P | C10 | AD_P<5> | HA06_P | K10 | CD_P<5> | HB06_P_CC | K28 | DD_P<5> |
| LA07_N | H14 | AD_N<6> | HA07_N | J10 | CD_N<6> | HB07_N | J28 | DD_N<6> |
| LA07_P | H13 | AD_P<6> | HA07_P | J9 | CD_P<6> | HB07_P | J27 | DD_P<6> |
| LA08_N | G13 | AD_N<7> | HA08_N | F11 | CD_N<7> | HB08_N | F29 | DD_N<7> |
| LA08_P | G12 | AD_P<7> | HA08_P | F10 | CD_P<7> | HB08_P | F28 | DD_P<7> |
| LA09_N | D15 | AD_N<8> | HA09_N | E10 | CD_N<8> | HB09_N | E28 | DD_N<8> |
| LA09_P | D14 | AD_P<8> | HA09_P | E9 | CD_P<8> | HB09_P | E27 | DD_P<8> |
| LA10_N | C15 | AD_N<9> | HA10_N | K14 | CD_N<9> | HB10_N | K32 | DD_N<9> |
| LA10_P | C14 | AD_P<9> | HA10_P | K13 | CD_P<9> | HB10_P | K31 | DD_P<9> |
| LA11_N | H17 | N.C. | HA11_N | J13 | N.C. | HB11_N | J31 | N.C. |
| LA11_P | H16 | N.C. | HA11_P | J12 | N.C. | HB11_P | J30 | N.C. |
| LA12_N | G16 | N.C. | HA12_N | F14 | N.C. | HB12_N | F32 | N.C. |
| LA12_P | G15 | N.C. | HA12_P | F13 | N.C. | HB12_P | F31 | N.C. |
| LA13_N | D18 | N.C. | HA13_N | E13 | N.C. | HB13_N | E31 | N.C. |
| LA13_P | D17 | N.C. | HA13_P | E12 | N.C. | HB13_P | E30 | N.C. |
| LA14_N | C19 | N.C. | HA14_N | J16 | N.C. | HB14_N | K35 | N.C. |
| LA14_P | C18 | N.C. | HA14_P | J15 | N.C. | HB14_P | K34 | N.C. |
| LA15_N | H20 | N.C. | HA15_N | F17 | N.C. | HB15_N | J34 | N.C. |
| LA15_P | H19 | N.C. | HA15_P | F16 | N.C. | HB15_P | J33 | N.C. |
| LA16_N | G19 | N.C. | HA16_N | E16 | N.C. | HB16_N | F35 | N.C. |
| LA16_P | G18 | N.C. | HA16_P | E15 | N.C. | HB16_P | F34 | N.C. |
| LA17_N_CC | D21 | BDR_N | HA17_N_CC | K17 | COR_N | HB17_N_CC | K38 | DOR_N |
| LA17_P_CC | D20 | BDR_P | HA17_P_CC | K16 | COR_P | HB17_P_CC | K37 | DOR_P |
| LA18_N_CC | C23 | BD_N<0> | HA18_N | J19 | N.C. | HB18_N | J37 | N.C. |
| LA18_P_CC | C22 | BD_P<0> | HA18_P | J18 | N.C. | HB18_P | J36 | N.C. |
| LA19_N | H23 | BD_N<1> | HA19_N | F20 | AOR_N | HB19_N | E34 | FMC_TO_CPLD<3> |
| LA19_P | H22 | BD _P<1> | HA19_P | F19 | AOR_P | HB19_P | E33 | FMC_TO_CPLD<2> |
| LA20_N | G22 | BD_N<2> | HA20_N | E19 | N.C. | HB20_N | F38 | FRONT_IO_FMC<1> |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LA20_P | G21 | BD_P<2> | HA20_P | E18 | N.C. | HB20_P | F37 | FRONT_IO_FMC<0> |
| LA21_N | H26 | BD_N<3> | HA21_N | K20 | BOR_N | HB21_N | E37 | FRONT_IO_FMC<3> |
| LA21_P | H25 | BD_P<3> | HA21_P | K19 | BOR_P | HB21_P | E36 | FRONT_IO_FMC<2> |
| LA22_N | G25 | BD_N<4> | HA22_N | J22 | N.C. | | | |
| LA22_P | G24 | BD_P<4> | HA22_P | J21 | N.C. | | | |
| LA23_N | D24 | BD_N<5> | HA23_N | K23 | FMC_TO_CPLD<1> | SCL | C30 | I2C_SCL |
| LA23_P | D23 | BD_P<5> | HA23_P | K22 | FMC_TO_CPLD<0> | SDA | C31 | I2C_SDA |
| LA24_N | H29 | BD_N<6> | DP0_C2M_N | C3 | DP_C2M_N<0> | DP0_M2C_N | C7 | DP_M2C_N<0> |
| LA24_P | H28 | BD_P<6> | DP0_C2M_P | C2 | DP_C2M_P<0> | DP0_M2C_P | C6 | DP_M2C_P<0> |
| LA25_N | G28 | BD_N<7> | DP1_C2M_N | A23 | DP_C2M_N<1> | DP1_M2C_N | A3 | DP_M2C_N<1> |
| LA25_P | G27 | BD_P<7> | DP1_C2M_P | A22 | DP_C2M_P<1> | DP1_M2C_P | A2 | DP_M2C_P<1> |
| LA26_N | D27 | BD_N<8> | DP2_C2M_N | A27 | DP_C2M_N<2> | DP2_M2C_N | A7 | DP_M2C_N<2> |
| LA26_P | D26 | BD_P<8> | DP2_C2M_P | A26 | DP_C2M_P<2> | DP2_M2C_P | A6 | DP_M2C_P<2> |
| LA27_N | C27 | BD_N<9> | DP3_C2M_N | A31 | DP_C2M_N<3> | DP3_M2C_N | A11 | DP_M2C_N<3> |
| LA27_P | C26 | BD_P<9> | DP3_C2M_P | A30 | DP_C2M_P<3> | DP3_M2C_P | A10 | DP_M2C_P<3> |
| LA28_N | H32 | N.C. | DP4_C2M_N | A35 | DP_C2M_N<4> | DP4_M2C_N | A15 | DP_M2C_N<4> |
| LA28_P | H31 | N.C. | DP4_C2M_P | A34 | DP_C2M_P<4> | DP4_M2C_P | A14 | DP_M2C_P<4> |
| LA29_N | G31 | N.C. | DP5_C2M_N | A39 | DP_C2M_N<5> | DP5_M2C_N | A19 | DP_M2C_N<5> |
| LA29_P | G30 | N.C. | DP5_C2M_P | A38 | DP_C2M_P<5> | DP5_M2C_P | A18 | DP_M2C_P<5> |
| LA30_N | H35 | N.C. | DP6_C2M_N | B37 | DP_C2M_N<6> | DP6_M2C_N | B17 | DP_M2C_N<6> |
| LA30_P | H34 | N.C. | DP6_C2M_P | B36 | DP_C2M_P<6> | DP6_M2C_P | B16 | DP_M2C_P<6> |
| LA31_N | G34 | N.C. | DP7_C2M_N | B33 | DP_C2M_N<7> | DP7_M2C_N | B13 | DP_M2C_N<7> |
| LA31_P | G33 | N.C. | DP7_C2M_P | B32 | DP_C2M_P<7> | DP7_M2C_P | B12 | DP_M2C_P<7> |
| LA32_N | H38 | N.C. | DP8_C2M_N | B29 | DP_C2M_N<8> | DP8_M2C_N | B9 | DP_M2C_N<8> |
| LA32_P | H37 | N.C. | DP8_C2M_P | B28 | DP_C2M_P<8> | DP8_M2C_P | B8 | DP_M2C_P<8> |
| LA33_N | G37 | N.C. | DP9_C2M_N | B25 | DP_C2M_N<9> | DP9_M2C_N | B5 | DP_M2C_N<9> |
| LA33_P | G36 | N.C. | DP9_C2M_P | B24 | DP_C2M_P<9> | DP9_M2C_P | B4 | DP_M2C_P<9> |

**Table 11: FMC126 signal description**

| Signal | Group | Direction | I/O standard | Description |
|---|---|---|---|---|
| ADR_N<br>ADR_P | A/D A | Output | LVDS | Digital data clock from ADC. |
| AD_N<9..0><br>AD_P<9..0> | A/D A | Output | LVDS | Data port, data is valid on both edges of the clock (DDR) |
| AOR_N<br>AOR_P | A/D A | Output | LVDS | Over-range bit synchronous to the samples present on data port |
| BDR_N<br>BDR_P | A/D B | Output | LVDS | Digital data clock from ADC. |
| BD_N<9..0><br>BD_P<9..0> | A/D B | Output | LVDS | Data port, data is valid on both edges of the clock (DDR) |
| BOR_N<br>BOR_P | A/D B | Output | LVDS | Over-range bit synchronous to the |

| | | | | |
|---|---|---|---|---|
| | | | | samples present on data port |
| CDR_N<br>CDR_P | A/D C | Output | LVDS | Digital data clock from ADC. |
| CD_N<9..0><br>CD_P<9..0> | A/D C | Output | LVDS | Data port, data is valid on both edges of the clock (DDR) |
| COR_N<br>COR_P | A/D C | Output | LVDS | Over-range bit synchronous to the samples present on data port |
| DDR_N<br>DDR_P | A/D D | Output | LVDS | Digital data clock from ADC. |
| DD_N<9..0><br>DD_P<9..0> | A/D D | Output | LVDS | Data port, data is valid on both edges of the clock (DDR) |
| DOR_N<br>DOR_P | A/D D | Output | LVDS | Over-range bit synchronous to the samples present on data port |
| CLK_TO_FPGA_N<br>CLK_TO_FPGA_P | MONITOR | Output | LVDS | Spare clock signal from the clock tree. Can be used to monitor onboard/external clock. |
| TRIGGER_TO_FPGA_N<br>TRIGGER_TO_FPGA_P | I/O | Output | LVDS | Representation of the signal connected to the external trigger input. |
| FRONT_IO<3..0> | I/O | Bidir | CMOS VADJ | Connected to the transceivers on the HDMI connector (Table 2). The direction of the transceivers is controlled through a CPLD register. |
| DP_M2C_P/N<1..0> | O | Output | CML/ECL | Gigabit transceiver from HDMI connector |
| DP_C2M_P/N<3..2> | I | Input | CML/ECL | Gigabit transceiver to HDMI connector |
| SYNC_FROM_FPGA_N<br>SYNC_FROM_FPGA_P | CONTROL | Input | LVDS | Signal used to apply a sync pulse to both ADC in order to align the digital outputs on sample basis. |
| FMC_TO_CPLD<3..0> | CONTROL | Bidir | CMOS VADJ | Reserved. |
| I2C_SCL | CONTROL | Input | LVTTL 3.3V | I2C Clock. The I2C bus is the main control bus. |
| I2C_SDA | CONTROL | Bidir | LVTTL 3.3V | I2C Data. The I2C bus is the main control bus. |

# Appendix D CPLD Register map

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Name | '0' | ADCR | CLKR | SYNCSRC | | CLKSRC | | |

**Table 12: Register CPLD_REG0 definition**

| Field | | Description |
|---|---|---|
| **CLKSRC** | | **Selection of clock source** |
| | '000' | External clock |
| | '011' | Internal clock, External Reference |
| | '110' | Internal clock, Internal Reference |
| | others | Do not use |
| **SYNCSRC** | | **Selection of synchronisation source** |
| | '00' | External Trigger |
| | '01' | Carrier (trough SYNC_FROM_FPGA_P/N) |
| | '10' | Clock Tree |
| | '11' | No Sync |
| **CLKR** | | **Clock tree SPI reset** |
| | '0' | Normal operation |
| | '1' | Reset, resetting the clock tree is normally not required. This bit is **not** self-clearing. |
| **ADCR** | | **A/D device SPI reset** |
| | '0' | Normal operation |
| | '1' | Reset, resetting the A/D device is normally not required. This bit is **not** self-clearing. |

**Table 13 Register CPLD_REG0 description**

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Name | Rsvd | | FAN1 | FAN0 | DIR3 | DIR2 | DIR1 | DIR0 |

**Table 14: Register CPLD_REG1 definition**

| Field | | Description |
|---|---|---|
| **DIRx** | | Direction of Front IO transceiver (x = 0 to 3) |
| | ‘0’ | Signal x is input (FMC12X is receiver) |
| | ‘1’ | Signal x is output (FMC12X is transmitter) |
| **FANx** | | Power control for FAN header (x = 0 to 1) |
| | ‘0‘ | Apply power to FAN header x |
| | ‘1‘ | Cut power to FAN header x |

**Table 15 Register CPLD_REG1 description**

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | Reserved | | | IRQ | VM | STATUS | LD | REFMON |

**Table 16: Register CPLD_REG2 definition (read)**

| Field | | Description |
|---|---|---|
| **REFMON** | | Reflect the status of the REFMON output of the AD9517 |
| **LD** | | Reflect the status of the LD output of the AD9517 |
| **STATUS** | | Reflect the status of the STATUS output of the AD9517 |
| **VM** | | Reflect the status of the INT# output of the ADT7411 (inverted) |
| | ‘0‘ | INT# is not asserted |
| | ‘1‘ | INT# is asserted, access to the ADT7411 trough the $I^2C$ bus is required to determine the source of the interrupt |
| **IRQ** | | Logic function: **NOT** (REFMON **AND** LD **AND** STATUS **AND** INT#) |
| | ‘0‘ | All status signals indicate OK |
| | ‘1‘ | One or more status signals indicate ERROR |

**Table 17 Register CPLD_REG2 description (read)**

| Bit nr. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **Name** | Reserved | | | LED_SEL | | | | |

**Table 18: Register CPLD_REG2 definition (write)**

| Field | | Description |
|---|---|---|
| **LED_SEL** | | Writing to this register determines which status signal is reflected on the LED. |
| | 'XXXX1' | REFMON |
| | 'XXX10' | LD |
| | 'XX100' | STATUS |
| | 'X1000' | VM |
| | '10000' | IRQ |

**Table 19 Register CPLD_REG2 description (write)**